

000000000000

IMAGE INPUT
SIGNAL LINE
112

PIXEL SOURCE SIGNAL LINE SIDE
DRIVING CIRCUIT 115

FIXED POTENTIAL
LINE 114

PIXEL GATE SIGNAL LINE SIDE
DRIVING CIRCUIT 116

SENSOR VERTICAL DRIVING CIRCUIT 118

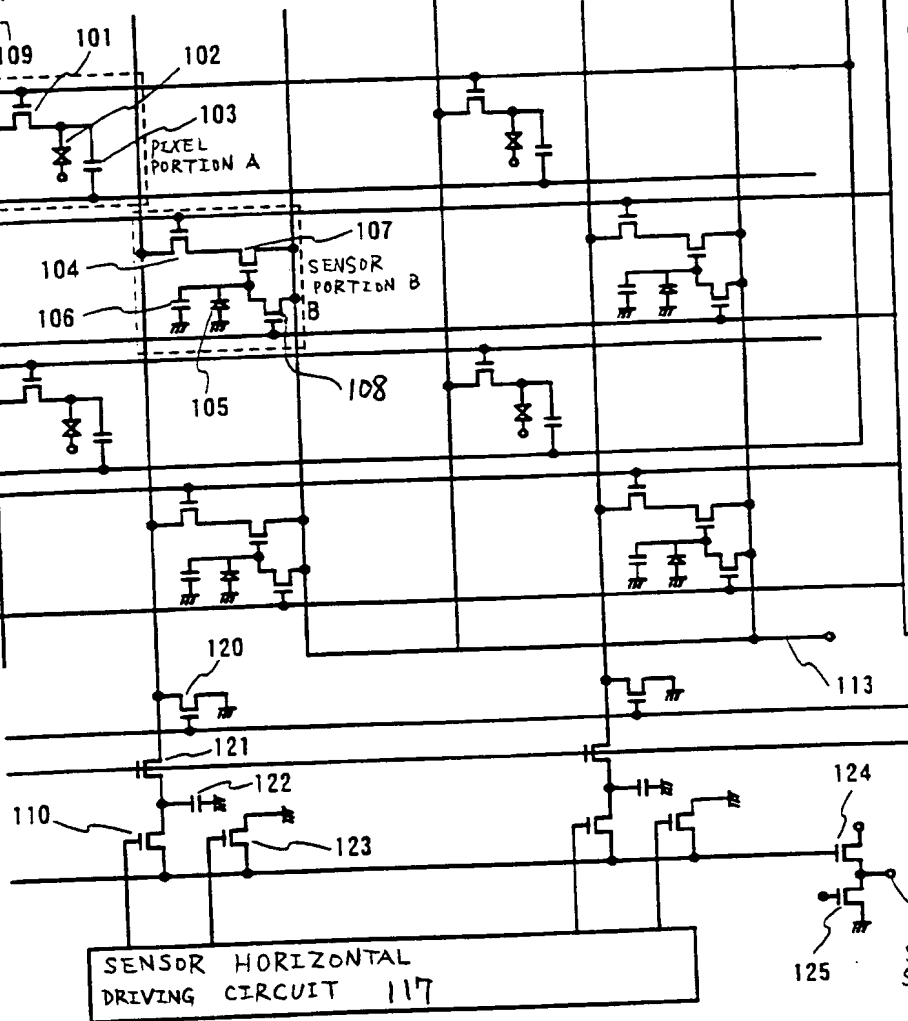


Fig. 1

00040470-024000

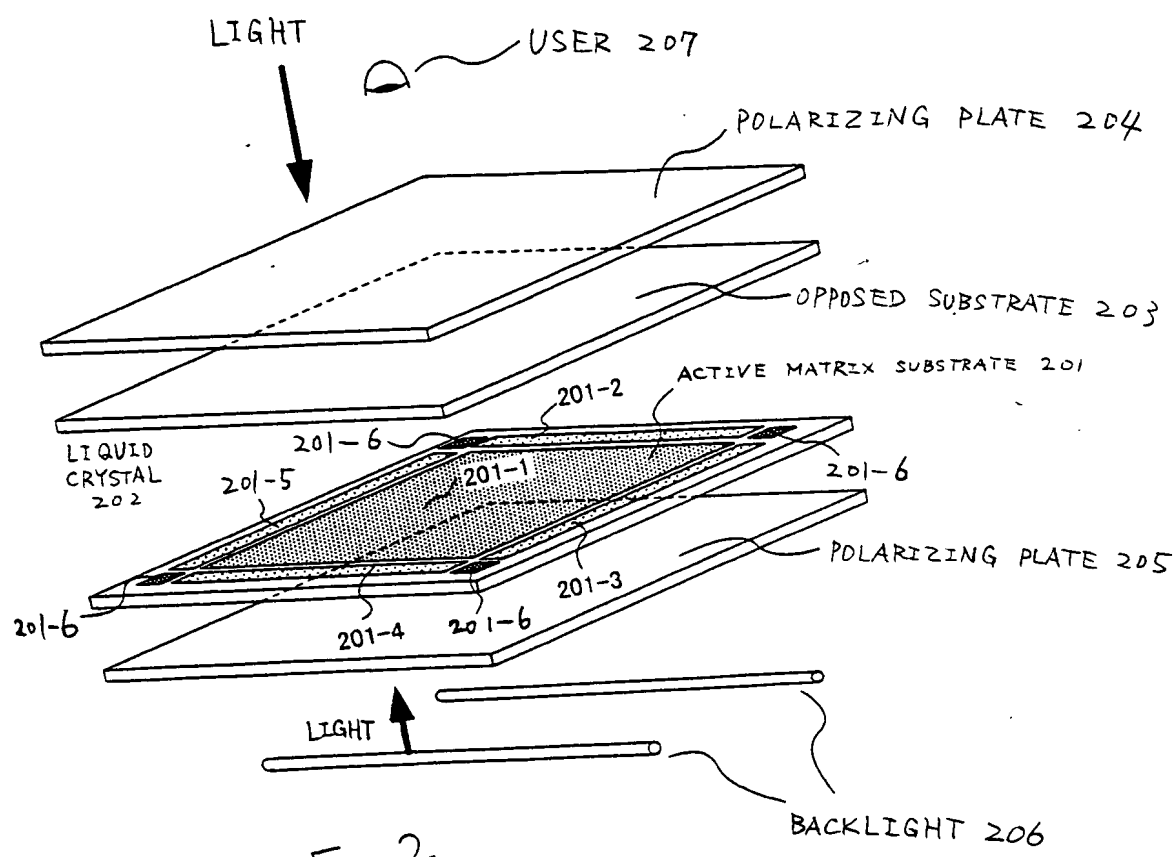


Fig. 2

005420-02461900

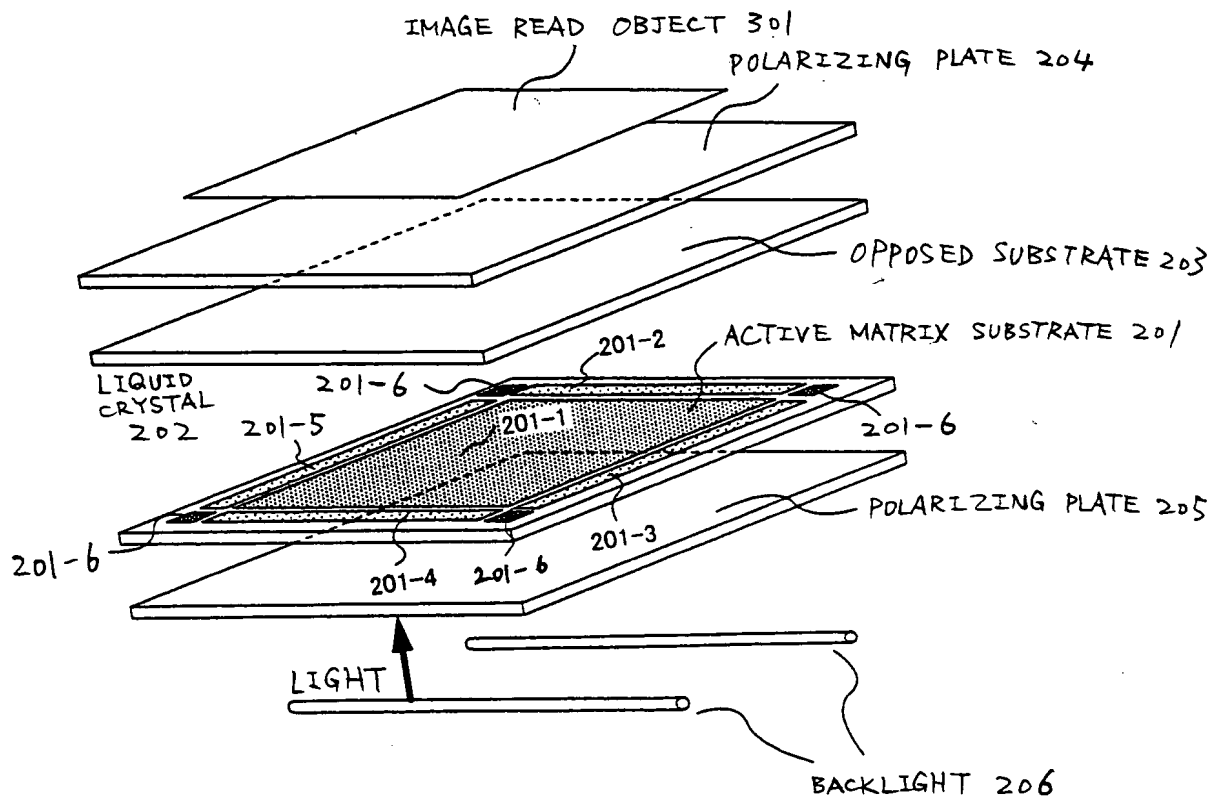


Fig. 3

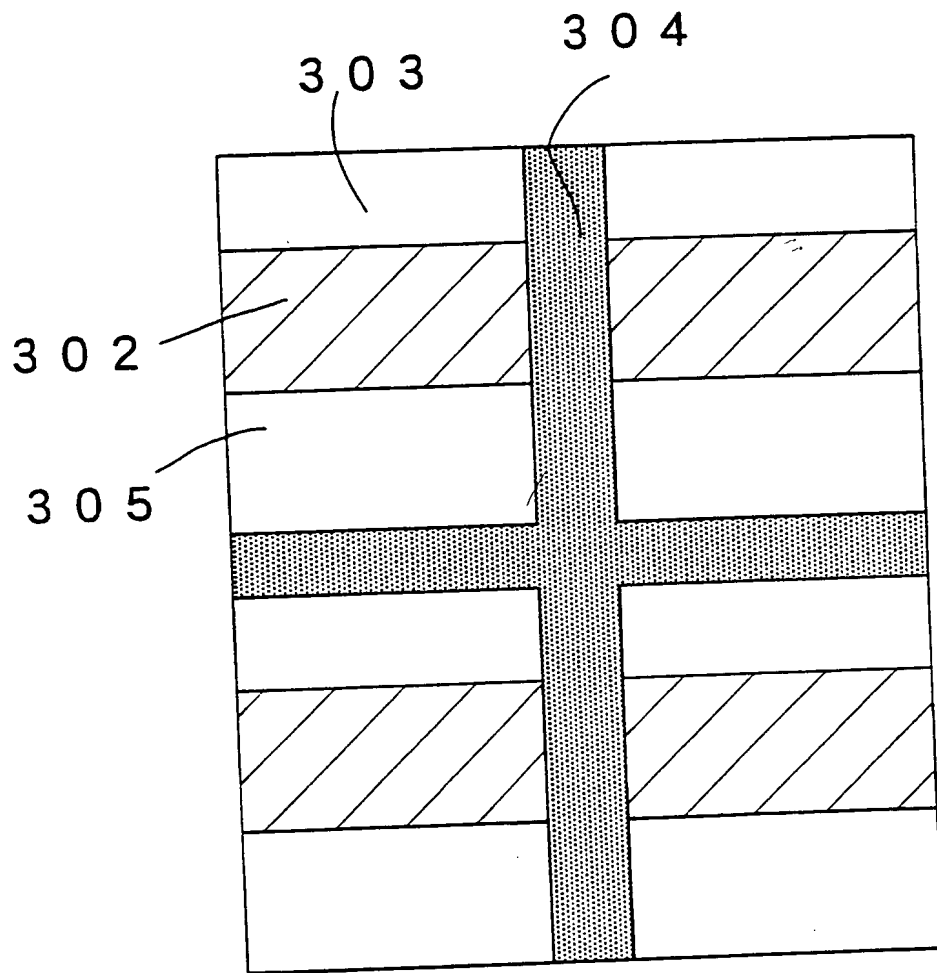


Fig. 4

SENSOR PORTION B

PIXEL PORTION A

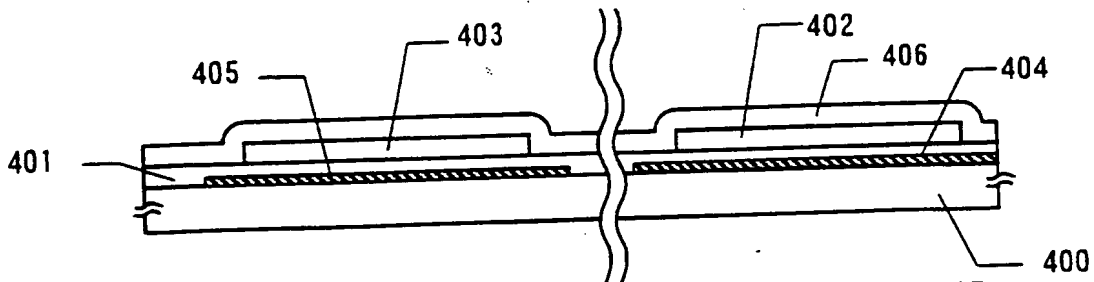


Fig. 6(A)

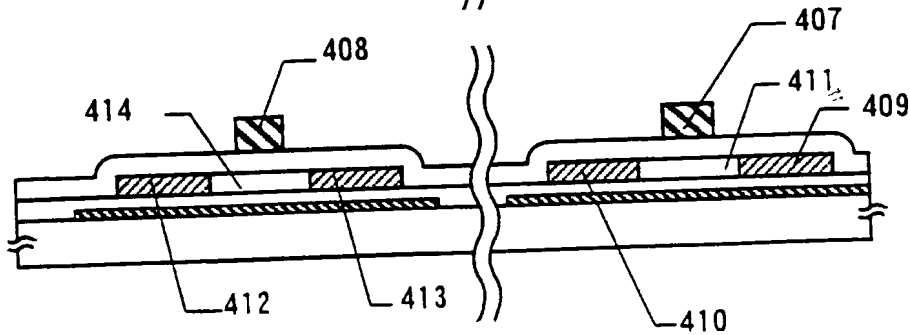


Fig. 6(B)

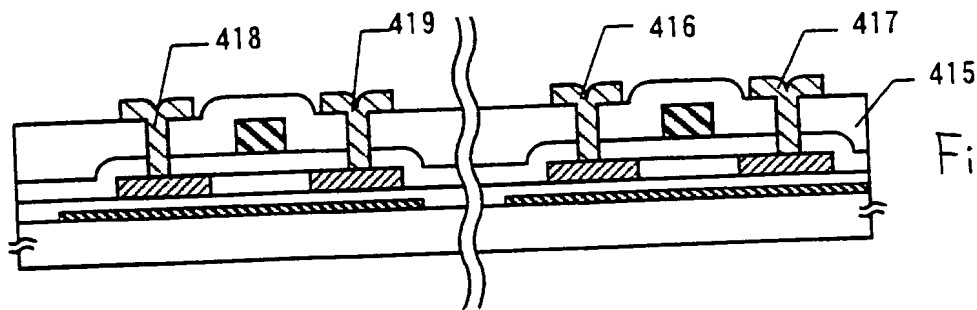


Fig. 6(C)

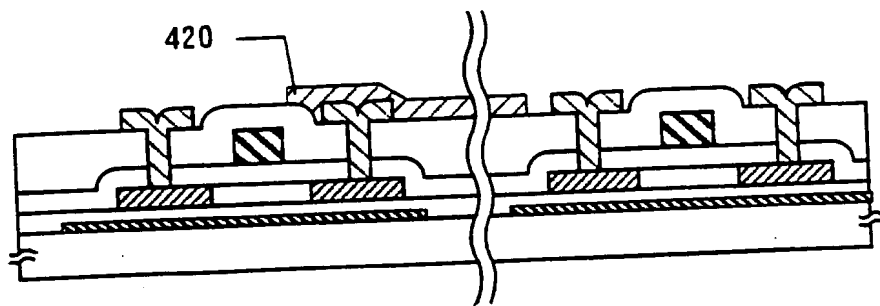


Fig. 6(D)

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SENSOR PORTION B

PIXEL PORTION A

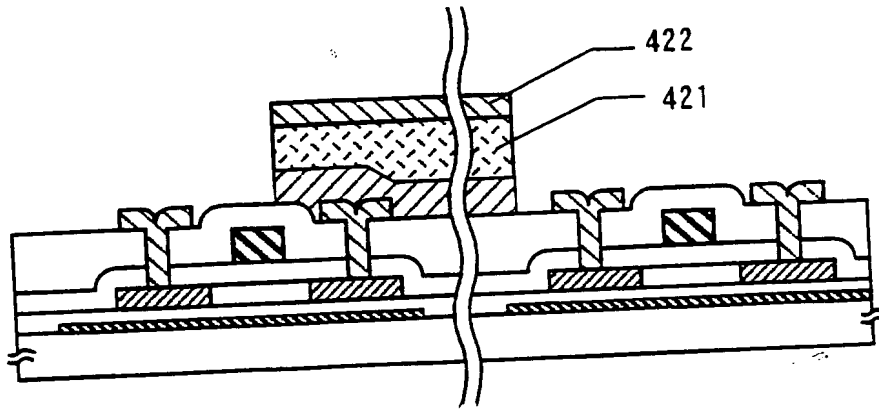


Fig. 7(A)

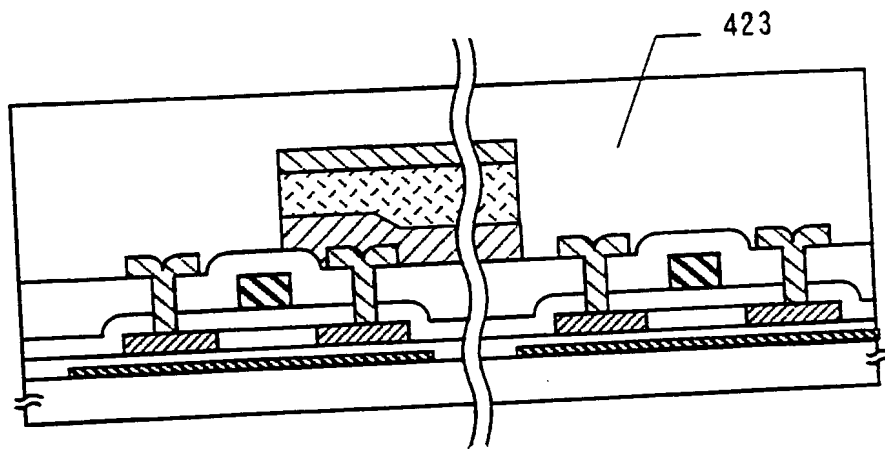


Fig. 7(B)

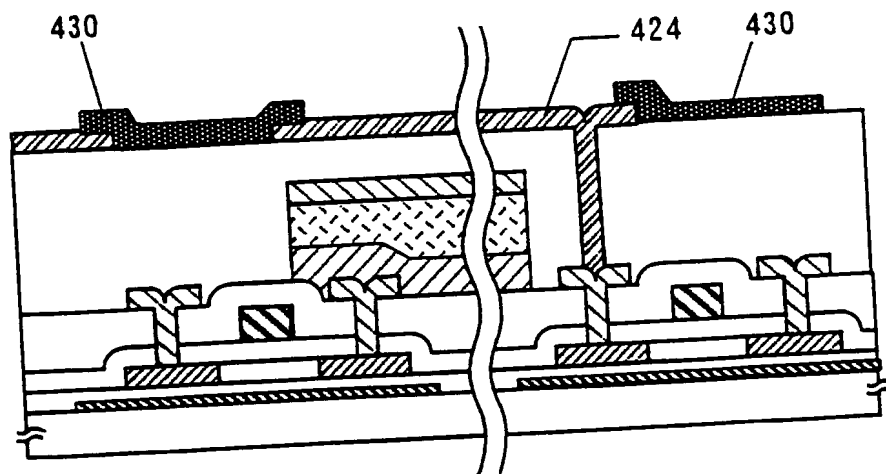
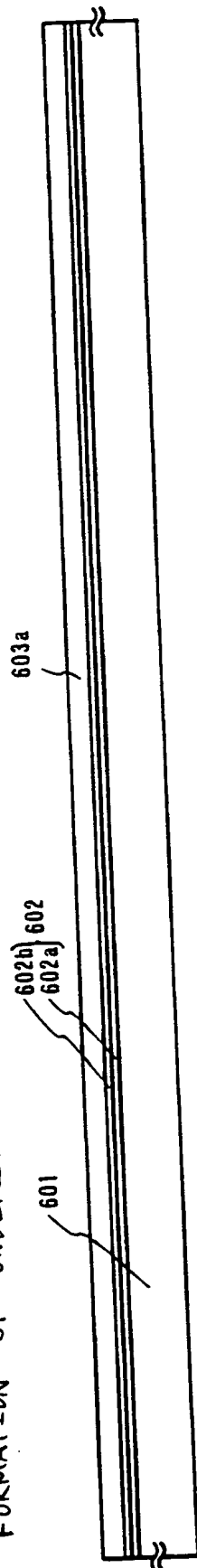


Fig. 7(C)

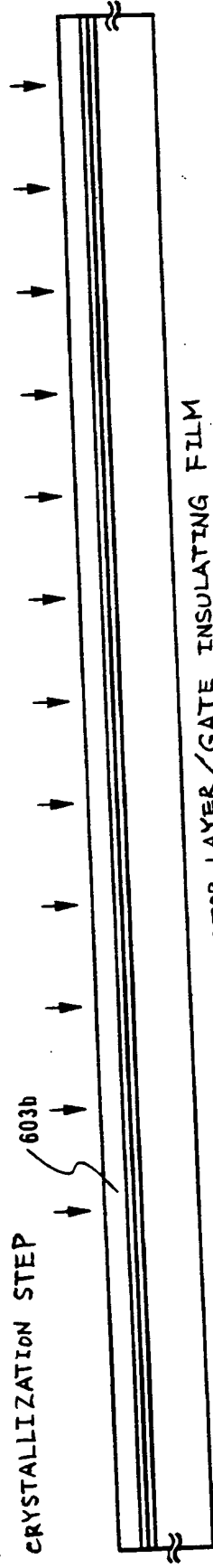
FORMATION OF UNDERLYING FILM / AMORPHOUS SEMICONDUCTOR FILM

Fig. 8(A)



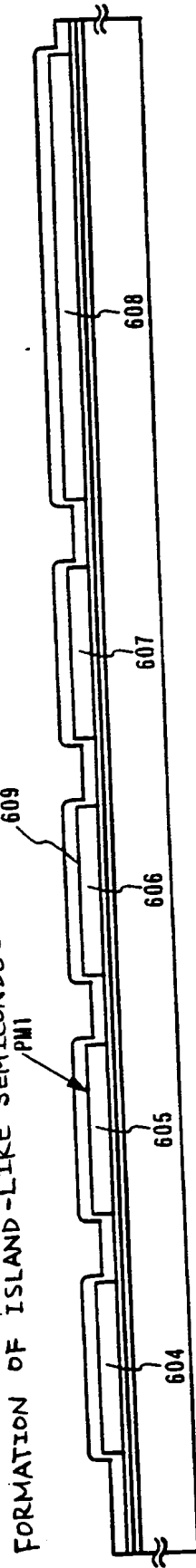
CRYSTALLIZATION STEP

Fig. 8(B)



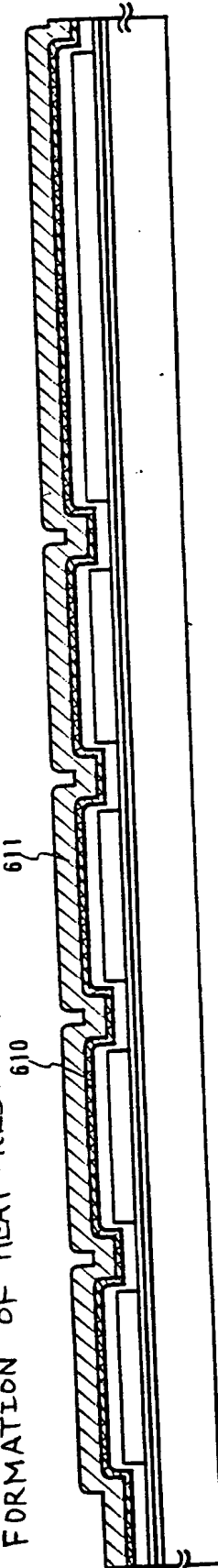
FORMATION OF ISLAND-LIKE SEMICONDUCTOR LAYER / GATE INSULATING FILM

Fig. 8(C)



FORMATION OF HEAT-RESISTANT CONDUCTOR LAYER

Fig. 8(D)



[illegible]

This diagram shows a cross-sectional view of a semiconductor device during a P^+ doping step. The device consists of a substrate with a thin layer of $PM4$ on top. A series of vertical arrows indicate the direction of the doping process. The device is divided into several regions, with labels 641, 642, and 643 indicating specific areas. The regions are separated by vertical lines, and the doping process is shown as a series of steps.

Fig. 10(A)

FORMATION OF PROTECTIVE INSULATION FILM

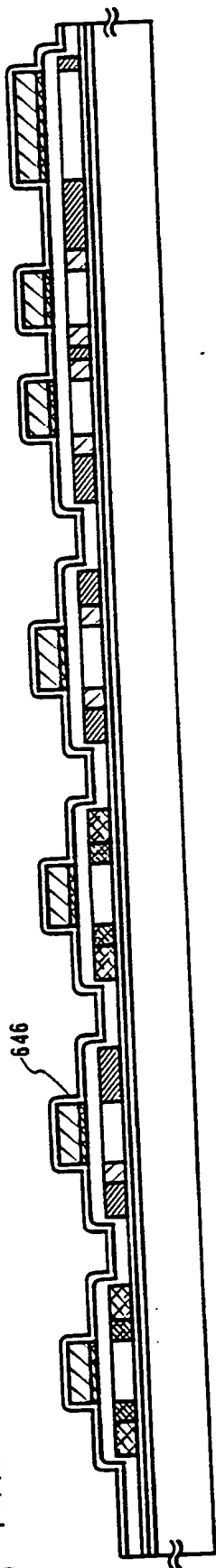


Fig. 10(B) ACTIVATION STEP

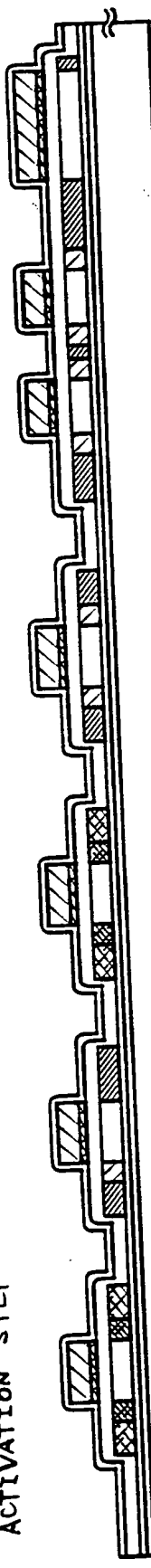
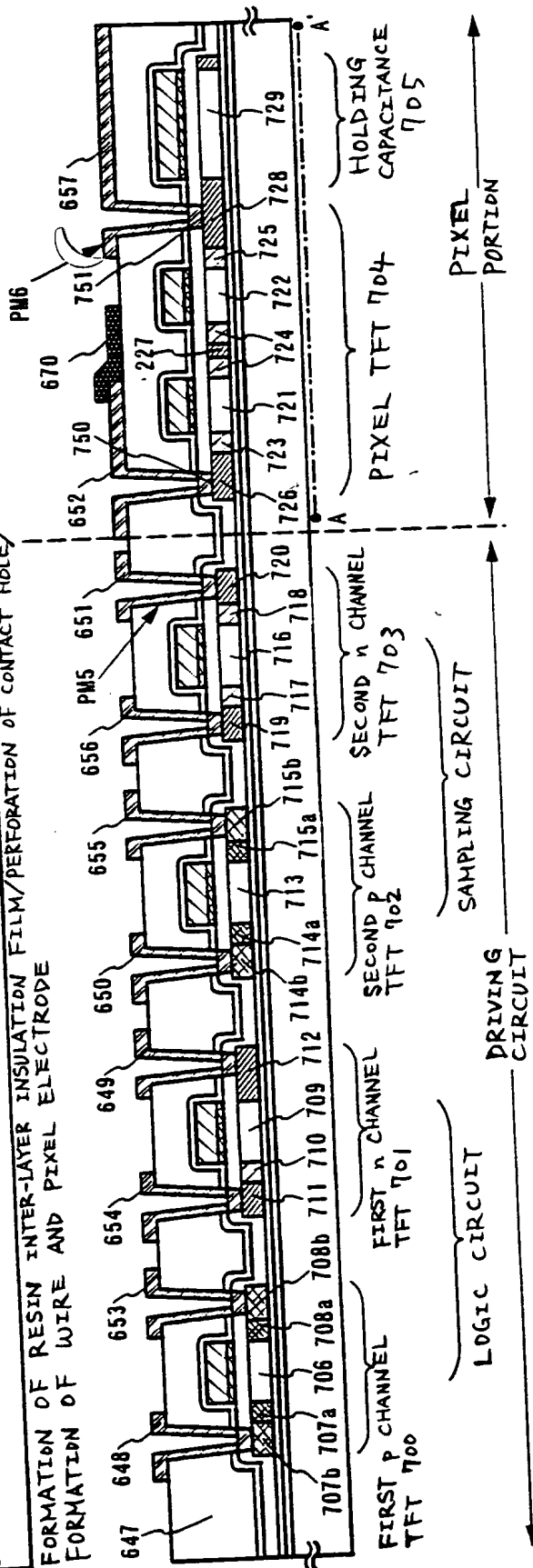


Fig. 10(c)

3. FORMATION OF RESIN INTER-LAYER INSULATION FILM/PERFORATION OF CONTACT HOLE/



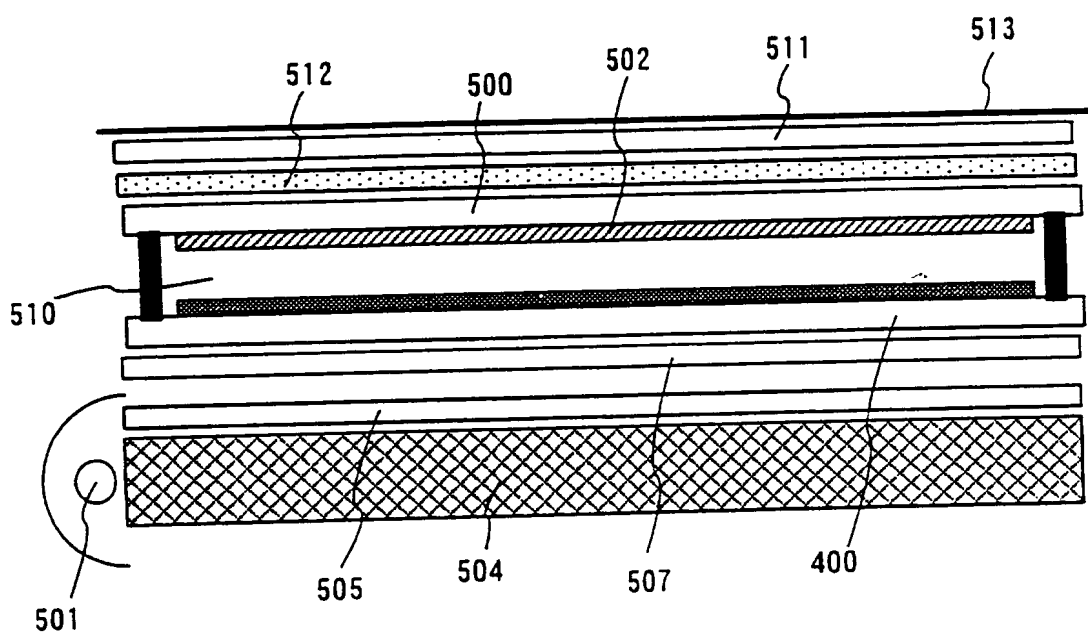


Fig. 11(A)

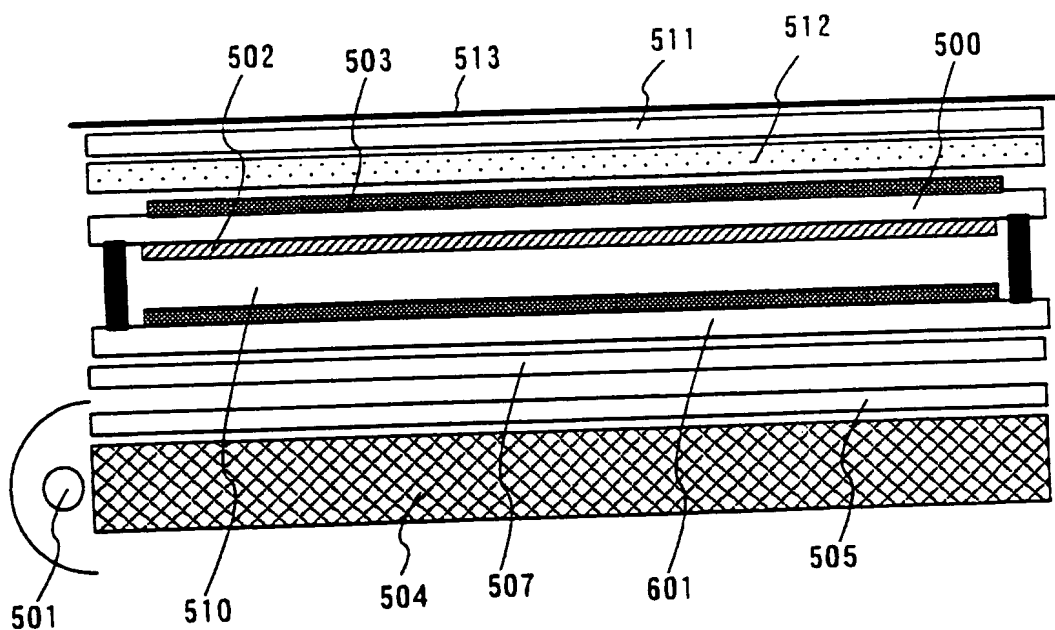


Fig. 11(B)

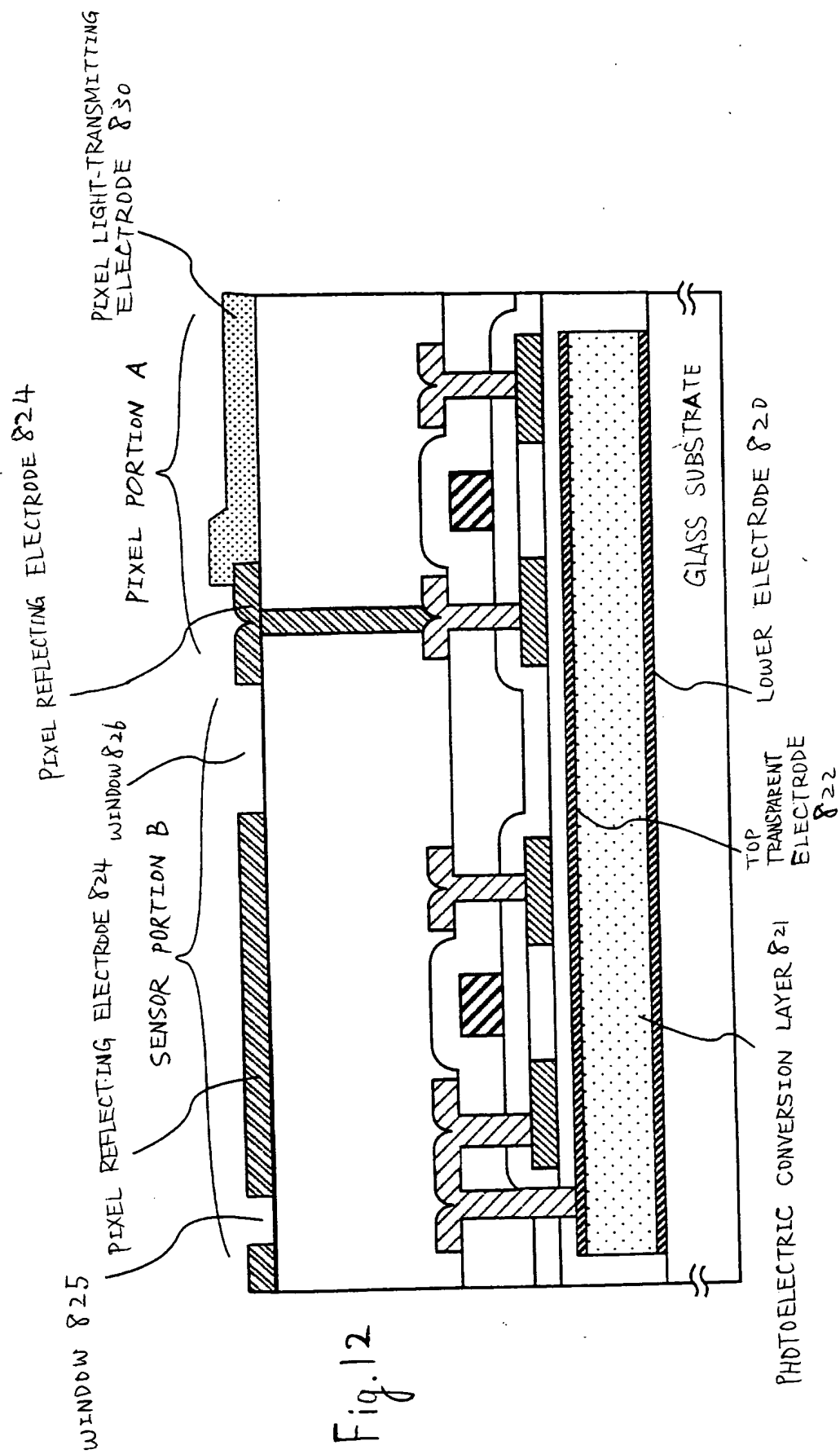


Fig. 12

112 IMAGE INPUT SIGNAL LINE

PIXEL SOURCE SIGNAL LINE SIDE
DRIVING CIRCUIT 115

FIXED POTENTIAL LINE 114

PIXEL GATE SIGNAL LINE SIDE
DRIVING CIRCUIT 116

SENSOR VERTICAL	DRIVING CIRCUIT	118
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SENSOR HORIZONTAL
DRIVING CIRCUIT 117

SENSOR OUTPUT
SIGNAL LINE III

Fig. 14